Elements Extraction of GaAs Dual-Gate MESFET Small-Signal Equivalent Circuit

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***Abstract*— A procedure for the extraction of intrinsic and extrinsic elements of dual-gate MESFET (DGMESFET) small-signal equivalent circuit is described in this paper. All the elements to be used as the initial values for the optimization calculation are extracted from dc and RF measurements with analytical formula. The elements of extrinsic series resistance are determined by considering the distributed channel resistance under the regions of two gates with the use of the "end resistance measurement" method. The elements of extrinsic capacitance and inductance are extracted by three-port Y-matrix and Z-matrix calculation from cold measurements. The intrinsic elements of DGMESFET, which is biased properly to be two decoupled single-gate MESFET's, are directly extracted from hot measurements. The extracted element values are then optimized to fit the resulting equivalent circuit to the measured three-port S-matrix. The developed procedure gives a practical and accurate approach for DGMESFET characterization.**

***Index Terms*—Dual-gate MESFET, equivalent circuit, parameter extraction.**

I. Introduction

THE equivalent circuit of a dual-gate MESFET (DGMESFET) is essential in the design of microwave circuits. The DGMESFET small-signal [l]–[3] and large-signal [4] models have been proposed by many authors. In general, a DGMESFET is basically modeled as a cascode circuit of two single-gate MESFET's (SGMESFET) [2] as shown in Fig. 1. The typical small-signal equivalent circuit of a coplanar DGMESFET, as shown in Fig. 2, contains two intrinsic FET's and extrinsic elements with a total of about 27 elements. Therefore, a straightforward optimization by fitting the element values of the equivalent circuit to the measured three-port S-matrix usually yields physically unacceptable results due to the calculation trapped into a local minimum. In addition, the port D_1 or S_2 connecting between two intrinsic FET's cannot be directly probed for measurement. It is then not easy to directly apply the analytical formula for the extraction of SGMESFET equivalent circuit elements [5] to the case of DGMESFET. In this paper, we develop a procedure for the extraction of extrinsic and intrinsic elements of a small-signal equivalent circuit of DGMESFET. The element values are initially extracted by dc and RF measurements using analytical formula. These values are then tweaked by optimization to yield accurate and correct results.

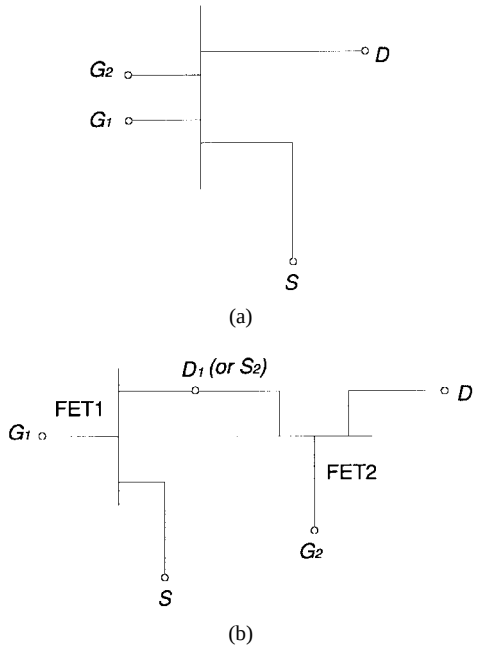

Fig. 1. Symbolic diagram of (a) a DGMESFET and (b) a cascode circuit of two SGMESFET's.

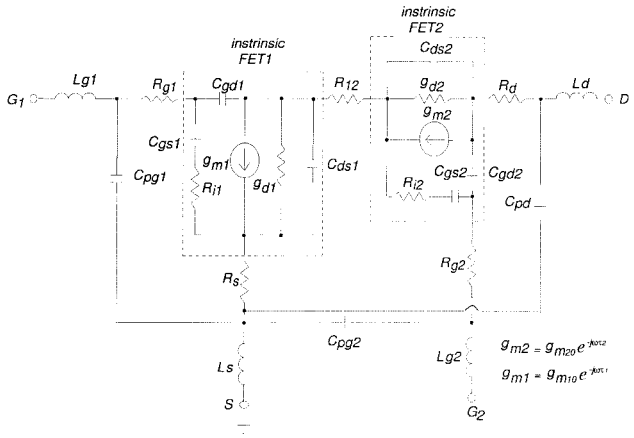

Fig. 2. A small-signal equivalent circuit of DGMESFET.

For a DGMESFET, the values of extrinsic series resistance can be estimated from physical modeling [1], [6] or derived by an empirical formula with the distributed channel resistance under the regions of two gates to be neglected [2], [3]. In this paper, a circuit model of a cold DGMESFET (i.e., $V_{DS} = 0$)

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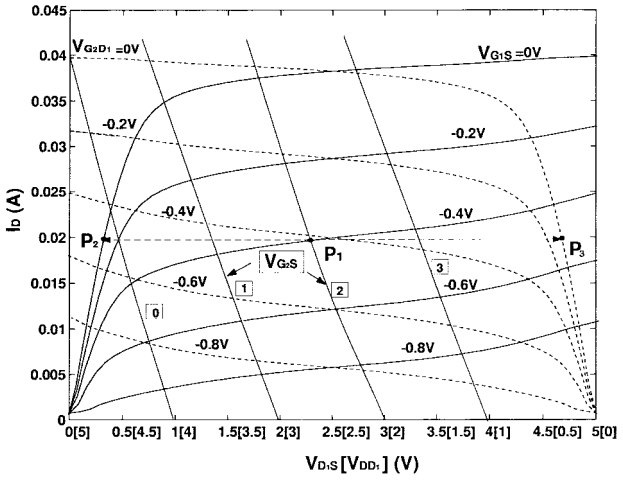

Fig. 3. Measured bidirection dc transfer characteristics of a GaAs DGMESFET with 1 μm gate length and 300 μm gate width for gates 1 and 2.

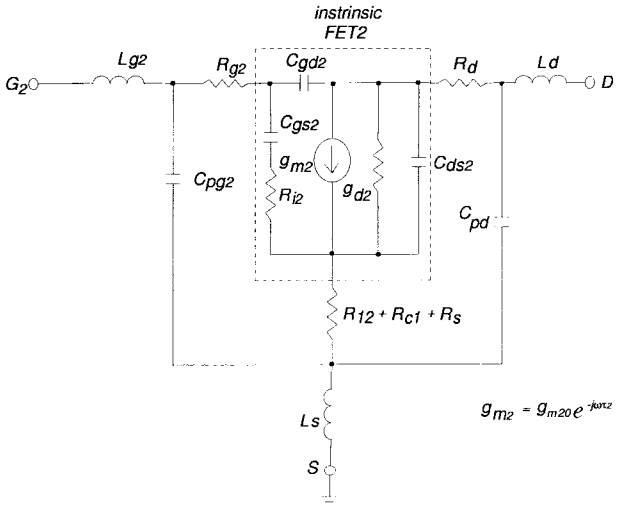

Fig. 4. Equivalent circuit of DGMESFET as biased at point P_2.

is proposed to consider the distributed channel resistance. The element values of extrinsic series resistance are then extracted by using the "end resistance measurement" method [7]. The extrinsic elements of capacitance and inductance are extracted using three-port Y-matrix and Z-matrix calculations from the cold measurements with the gate 1 or 2 of DGMESFET at forward bias or reverse bias accordingly. For the intrinsic elements, we use the DGMESFET bidirectional dc transfer characteristics to find the proper bias voltages for having one intrinsic FET in linear region and the other intrinsic FET in active region. This then allows us to derive the analytical formula for the intrinsic elements of DGMESFET.

In the following, Section II describes the extraction formula of DGMESFET intrinsic elements with the use of its dc transfer characteristics. In Section III, the extraction formula of extrinsic elements including series resistance, parasitic inductance, and capacitance are presented. The experimental results using the developed extraction procedure of an on-wafer coplanar DGMESFET are presented in Section IV. Finally, the conclusion is given in Section V.

II. Intrinsic Elements Extraction

A. DC Transfer Characteristics

Since DGMESFET is a cascode circuit of two single-gate FET's, its bidirection dc transfer characteristics $I_D(V_{G_1S}, V_{G_2S})|_{V_{DS}}$ can be derived using

$$V_{DS} = V_{D_1S} + V_{DD_1} \tag{1}$$

$$V_{G_2D_1} = V_{G_2S} - V_{D_1S} \tag{2}$$

with the dc transfer characteristics of two SGMESFET's [8]. Fig. 3 shows an example of the measured dc transfer characteristics of a DGMESFET with 1-μm gate length and 300-μm gate width. As P_1 is the bias point of DGMESFET with $V_{DS} = 5$ V, $V_{G_1S} = -0.4$ V, and $V_{G_2S} = 2$ V, it corresponds to $I_D = 19.8$ mA, $V_{G_2D_1} = -0.413$ V, $V_{D_1S} = 2.413$ V, and $V_{DD_1} = 2.587$ V. As one horizontally shifts the bias point of FET1 to P_2 by changing V_{G_1S} and V_{D_1S} with I_D unchanged, FET1 is operated in the linear region as a resistor. FET2 is, however, biased at the same V_{DS_2}, $V_{G_2S_2}$ and I_D as those for P_1 point by adjusting V_{DS} properly. FET2 is then in the same active region as that in the DGMESFET operation. This gives the operation of DGMESFET to be two decoupled SGMESFET's with FET2 bias condition unchanged and FET1 as a series resistor. It can simplify the intrinsic elements extraction to be described in the following. Note one can similarly shift the bias point of FET2 to P_3, and the operation of DGMESFET becomes a SGMESFET (FET1) in series with a resistor (FET2).

B. Intrinsic Elements

As described above, the dc transfer characteristics of DGMESFET can be decomposed into two cases. In each case, there is one FET operating as a resistor and the other FET is operating at the same dc biases as those in the DGMESFET operation. For example, as the biases change from P_1 to P_2, FET1 can be modeled by series resistance $R_s + R_{c1} + R_{12}$. Since the biases of FET2 are unchanged in the same active region as that in the DGMESFET operation, the three-port equivalent circuit can be reduced into a two-port equivalent circuit as shown in Fig. 4. Similarly, as the bias point is changed to P_3, FET2 is modeled by series resistance $R_{12} + R_{c2} + R_d$. FET1 is then in active region with the resulting two-port equivalent circuit as shown in Fig. 5.

Figs. 4 and 5 indicate that one can use the similar matrix manipulation as those for SGMESFET given in [5]. In other words, as the extrinsic elements are extracted, one can acquire the two-port Y-matrix from the measured two-port S-matrix. The intrinsic elements of FET1 and FET2 can then be determined analytically as follows:

$$C_{gdj} = \frac{\mathrm{Im}(Y_{12})}{\omega} \tag{3}$$

$$C_{gsj} = \frac{\mathrm{Im}(Y_{11} - \omega C_{gdj})}{\omega}\left(1 + \frac{(\mathrm{Re}(Y_{11}))^2}{(\mathrm{Im}(Y_{11}) - \omega C_{gdj})^2}\right) \tag{4}$$

$$R_{ij} = \frac{\mathrm{Re}(Y_{11})}{(\mathrm{Im}(Y_{11}) - \omega C_{gdj})^2 + (\mathrm{Re}(Y_{11}))^2} \tag{5}$$

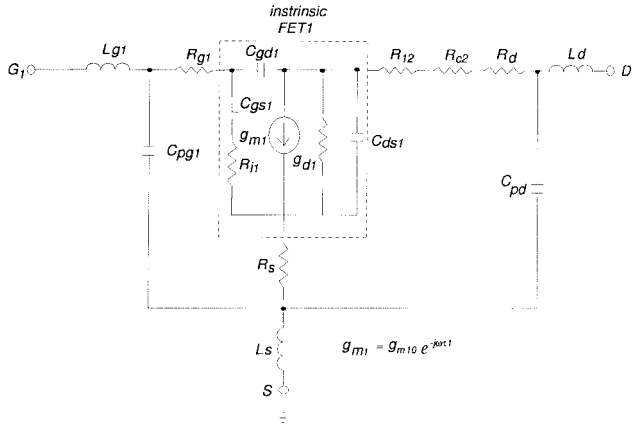

Fig. 5. Equivalent circuit of DGMESFET as biased at point P_3.

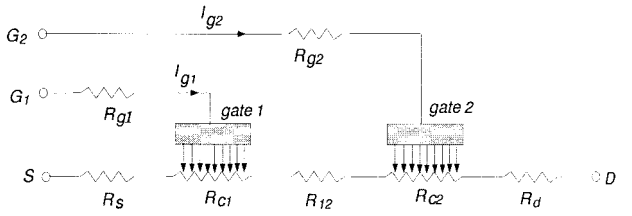

Fig. 6. Schematic diagram of DGMESFET for "end resistance measurement" method. R_{c1}, R_{c2} are the distributed channel resistance under the regions of gates 1 and 2, respectively. R_{12} is the bulk resistance between gates 1 and 2.

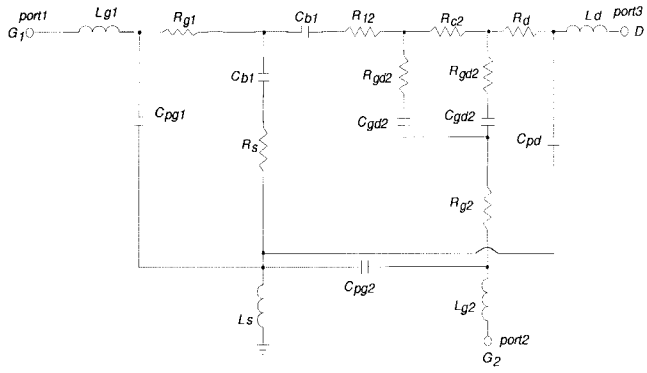

Fig. 7. Equivalent circuit of coplanar cold DGMESFET with FET1 reverse biased and FET2 forward biased.

$$g_{mj} = \sqrt{\Big((\mathrm{Re}(Y_{21}))^2+(\mathrm{Im}(Y_{21})+\omega C_{gdj})^2\Big)\big(1+\omega^2 C_{gsj}^2 R_{ij}^2\big)} \tag{6}$$

$$\tau_j = \frac{1}{\omega}\sin^{-1}\left(\frac{-\omega C_{gdj}-\mathrm{Im}(Y_{21})-\omega C_{gsj}R_{ij}\mathrm{Re}(Y_{21})}{g_{mj}}\right) \tag{7}$$

$$C_{dsj} = \frac{\mathrm{Im}(Y_{22})-\omega C_{gdj}}{\omega} \tag{8}$$

$$g_{dsj} = \mathrm{Re}(Y_{22}) \tag{9}$$

where $j = 1, 2$ for FET1 and FET2, respectively, Re and Im are the real part and imaginary part operators. In the following section, the formulas to extract the extrinsic elements are derived.

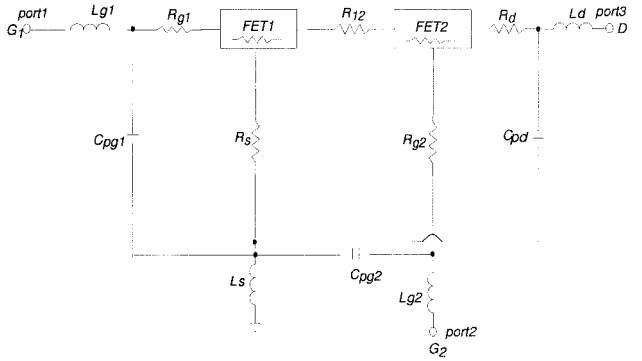

Fig. 8. Equivalent circuit of coplanar cold DGMESFET with FET1 and FET2 forward biased.

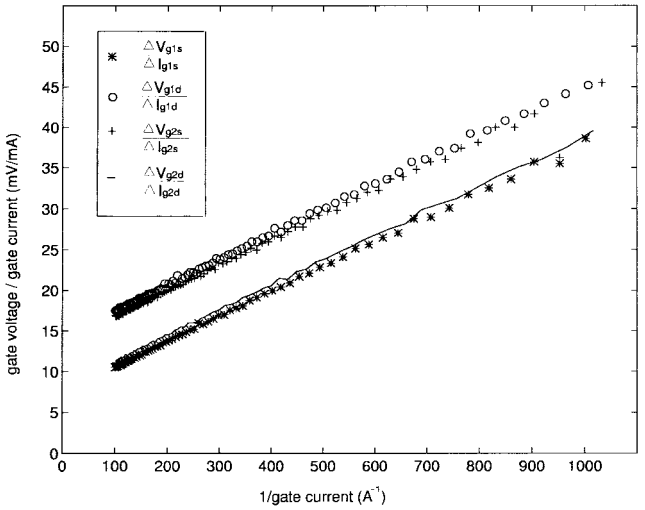

Fig. 9. Measured results of $(\Delta V_{g1s})/(\Delta I_{g1s})$, $(\Delta V_{g1d})/(\Delta I_{g1d})$, $(\Delta V_{g2s})/(\Delta I_{g2s})$, and $(\Delta V_{g2d})/(\Delta I_{g2d})$ at forward bias with drain terminal or source terminal floating.

III. Extrinsic Elements Extraction

A. Extrinsic Series Resistance

Fig. 6 describes the dc behavior of a cold DGMESFET with gates 1 or 2 under forward bias. The region under gates 1 or 2 is modeled as a uniform distributed resistive network. The current I_{g1} is then divided to be I_{g1s} to the source port and I_{g1d} to the drain port after it flows through the gate 1 region. Similarly, I_{g2} becomes I_{g2s} and I_{g2d} after it flows through the gate 2 region. Five independent equations can then be acquired from the "end resistance measurement" method [7]. They are given as

$$\frac{\Delta V_{g1s}}{\Delta I_{g1s}}\Big|_{\text{drain floating}} = R_{g1}+\frac{n_1 V_T}{I_{g1s}}+\frac{R_{c1}}{3}+R_s \tag{10}$$

$$\frac{\Delta V_{g2s}}{\Delta I_{g2s}}\Big|_{\text{drain floating}} = R_{g2}+\frac{n_2 V_T}{I_{g2s}}+\frac{R_{c2}}{3}+R_{12}+R_{c1}+R_s \tag{11}$$

$$\frac{\Delta V_{g2d}}{\Delta I_{g2d}}\Big|_{\text{source floating}} = R_{g2}+\frac{n_2 V_T}{I_{g2d}}+\frac{R_{c2}}{3}+R_d \tag{12}$$

$$\frac{\Delta V_{g1d}}{\Delta I_{g1d}}\Big|_{\text{source floating}} = R_{g1}+\frac{n_1 V_T}{I_{g1d}}+\frac{R_{c1}}{3}+R_{12}+R_{c2}+R_d \tag{13}$$

TABLE I
INITIAL AND FINAL VALUES OF THE DGMESFET EXTRINSIC AND INTRINSIC ELEMENTS

elements	inital values	final values
C_{gs1}	$0.2pF$	$0.22pF$
R_{i1}	7Ω	6.44Ω
g_{m10}	$0.058A/V$	$0.0618A/V$
τ_1	$7.6ps$	$7.2ps$
C_{gd1}	$63fF$	$64.3fF$
g_{d1}	$10mS$	$9.6mS$
C_{ds1}	$0.15pF$	$0.051pF$
C_{gs2}	$0.295pF$	$0.24pF$
R_{i2}	10Ω	9Ω
g_{m20}	$0.03A/V$	$0.025A/V$
τ_2	$8.04ps$	$7.7ps$
C_{gd2}	$68fF$	$60fF$
g_{d2}	$5.88mS$	$6.67mS$
C_{ds2}	$0.034pF$	$0.03pF$
R_{g1}	1.42Ω	1.32Ω
R_{g2}	1.04Ω	0.96Ω
R_s	4.86Ω	4.82Ω
R_d	4.81Ω	4.04Ω
R_{12}	3.06Ω	3.04Ω
C_{pg1}	$87fF$	$72fF$
C_{pg2}	$120fF$	$105fF$
C_{pd}	$58fF$	$57fF$
L_s	$0.001nH$	$0.001nH$
L_d	$0.089nH$	$0.095nH$
L_{g1}	$0.0186nH$	$0.0190nH$
L_{g2}	$0.0173nH$	$0.0168nH$

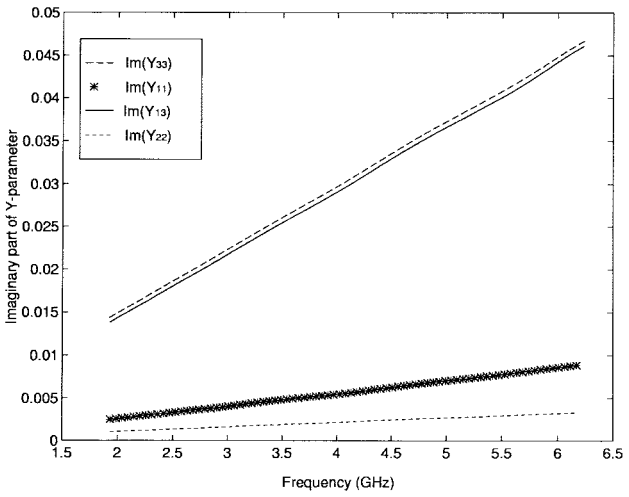

Fig. 10. Measured results of the imaginary part of three-port Y-matrix at $V_{ds} = O$ V, $V_{g1s} < V_{th}$, and $I_{g2s} = 1$ mA.

$$\frac{V_{ds}}{I_{g1s}}\Big|_{\text{drain floating}} = \frac{R_{c1}}{2} + R_s, \tag{14}$$

where n_1, n_2 are ideality factors of gates 1 and 2, V_T is the thermal potential.

Equation (10) shows a straight line for $V_{g1s} - I_{g1s}$ characteristics with $n_1 V_T$ as the slope and $R_{g1} + (R_{c1}/3) + R_s$ as the intercept point. Therefore, from a set of measurements of current I_{g1s} and voltage V_{g1s} with drain terminal floating, the

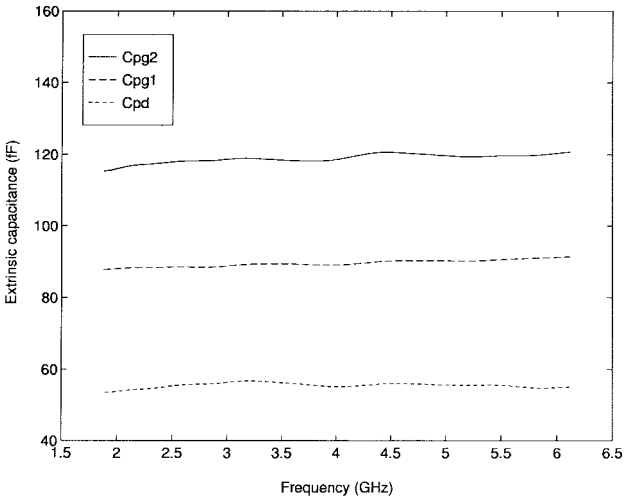

Fig. 11. Extracted results of extrinsic elements of capacitance.

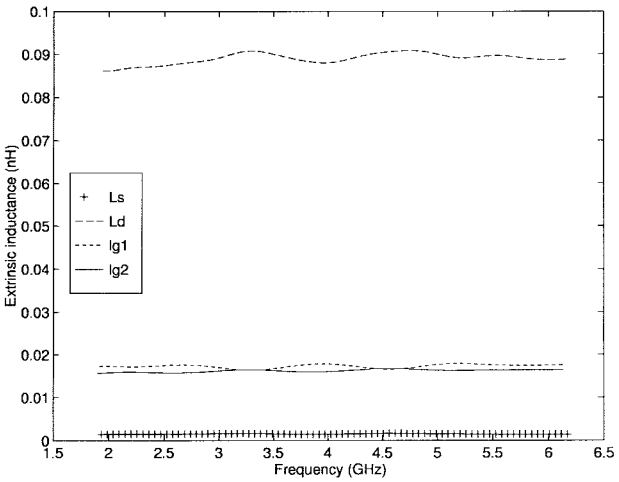

Fig. 12. Extracted results of extrinsic elements of inductance.

mean values of $(\Delta V_{g1s})/(\Delta I_{g1s})$ can be calculated to solve $n_1 V_T$ and $R_{g1} + (R_{c1}/3) + R_s$ by a least square error method. By using the same process, (10)–(13) become the following three-port Z-matrix expression:

$$R_{11} = R_{g1} + \frac{R_{c1}}{3} + R_s \tag{15}$$

$$R_{22} = R_{g2} + \frac{R_{c2}}{3} + R_{12} + R_{c1} + R_s \tag{16}$$

$$R_{32} = R_{g2} + \frac{R_{c2}}{3} + R_d \tag{17}$$

$$R_{31} = R_{g1} + \frac{R_{c1}}{3} + R_{12} + R_{c2} + R_d \tag{18}$$

and (14) can be rewritten as

$$R_x = \frac{R_{c1}}{2} + R_s. \tag{19}$$

To solve these seven extrinsic elements of series resistance, two additional equations can be selected using the following approaches.

1) The relation of R_{c1} and R_{c2}, $R_{c1} = mR_{c2}$, provided the gates 1 and 2 channel length ratio m is known.

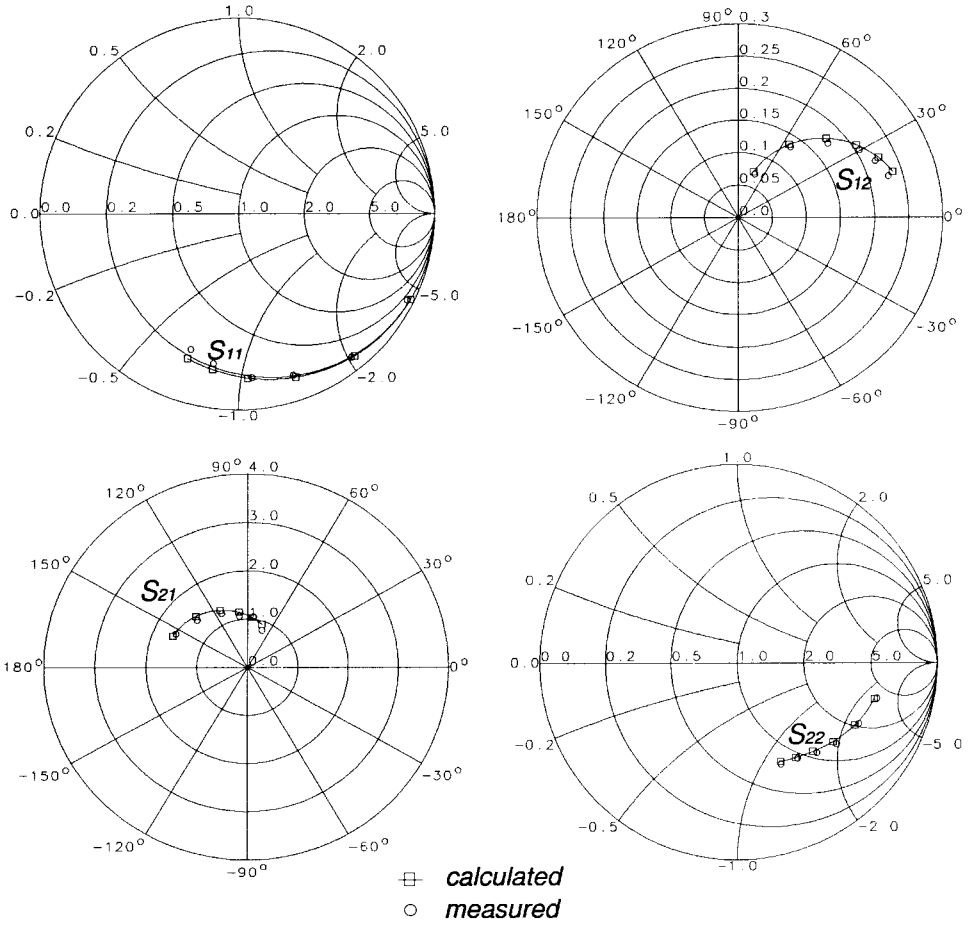

Fig. 13. Measured and calculated S-parameters of DGMESFET at bias point P_2 given in Fig. 3 with port 1: gate 2 and port 2: drain.

2) The value of $R_s+R_{12}+R_{c2}+R_d$ obtained from Hower and Bechtel method [9] by floating gate 2 terminal.
3) The values of R_{g1} and R_{g2} are acquired from dummy pad resistance measurement.
4) The values of R_s and R_d of SGMESFET [5] provided the same device structure and processing in DGMESFET for source and drain terminals.

Therefore, five extrinsic resistance elements including R_{g1}, R_{g2}, R_s, R_d, and R_{12} can be determined.

B. Extrinsic Capacitance

Fig. 7 shows the equivalent circuit of a cold coplanar DGMESFET in which FET1 is reverse biased in the pinch-off region and FET2 is forward biased in linear region. The imaginary part of its three-port Y-matrix, with frequency below a few gigahertz, can be written as

$$\mathrm{Im}(Y_{11}) = \omega(C_{pg1} + 2C_{b1}) \tag{20}$$
$$\mathrm{Im}(Y_{13}) = -\omega C_{b1} \tag{21}$$
$$\mathrm{Im}(Y_{22}) = \omega(2C_{gd2} + 2C_{pg2}) \tag{22}$$
$$\mathrm{Im}(Y_{23}) = -\omega 2C_{gd2} \tag{23}$$
$$\mathrm{Im}(Y_{33}) = \omega(C_{pd} + 2C_{gd2} + C_{b1}). \tag{24}$$

One can then solve the values of extrinsic capacitance C_{pg1}, C_{pg2}, C_{pd}, and C_{gd2} from the cold DGMESFET three-port S-matrix measurement using (20)–(24).

C. Extrinsic Inductance

Fig. 8 shows the equivalent circuit of a cold coplanar DGMESFET with FET1 and FET2 both at forward bias. FET1 and FET2 are then modeled by resistive networks. The imaginary part of its three-port Z-matrix, with frequency below a few gigahertz, can be written as

$$\mathrm{Im}(Z_{11}) = \omega(L_{g1} + L_s) \tag{25}$$
$$\mathrm{Im}(Z_{22}) = \omega(L_{g2} + L_s) \tag{26}$$
$$\mathrm{Im}(Z_{33}) = \omega(L_d + L_s) \tag{27}$$
$$\mathrm{Im}(Z_{21}) = \omega L_s. \tag{28}$$

One can then solve the values of extrinsic inductance L_{g1}, L_{g2}, L_s, and L_d from cold DGMESFET S-matrix measurement using (25)–(28).

Based on the approach described above, values of extrinsic and intrinsic elements can be determined using analytical formula from dc and RF measurements. These element values are then used as the initial values of a DGMESFET equivalent circuit for the optimization by fitting the resulting equivalent circuit to the measured three-port S-matrix. Several commercial high-frequency circuit simulators, such as HP/EESof, can be used for this optimization calculation. Since the optimization calculation is only used to tweak the element values, gradient search is suitable to minimize the

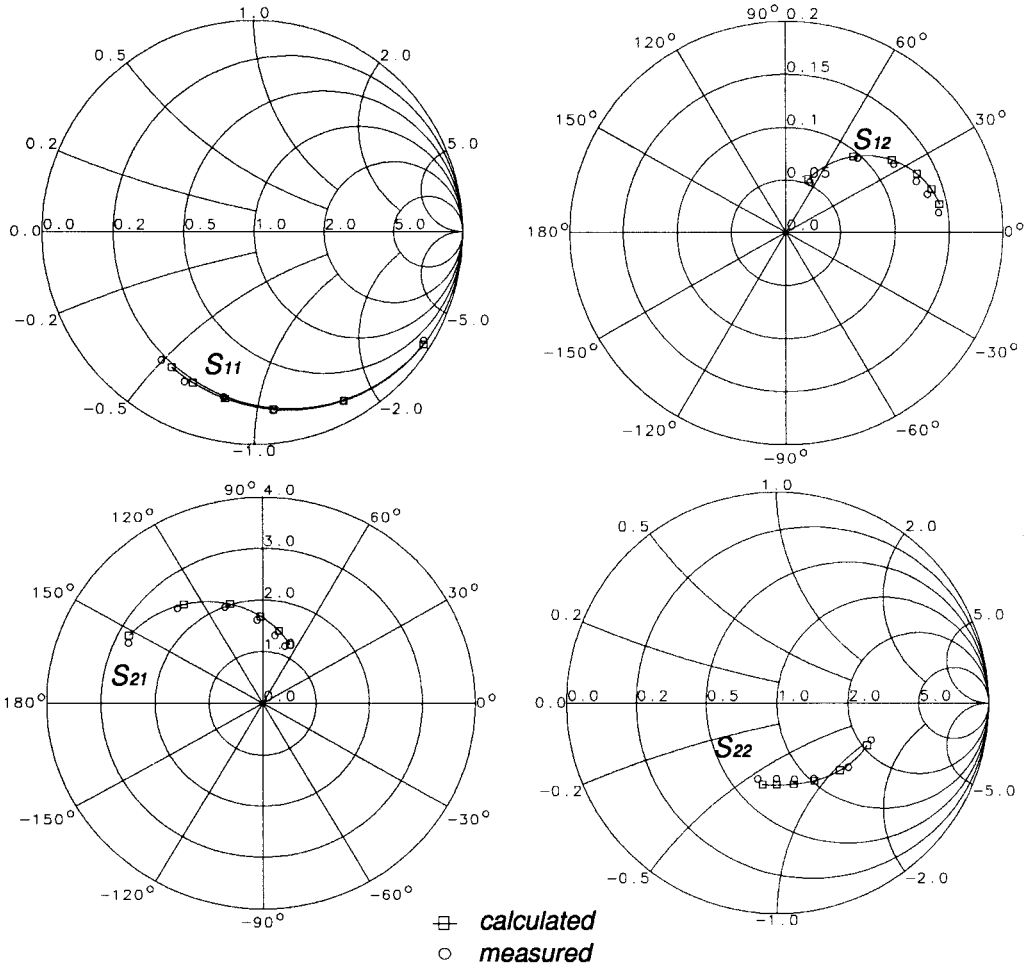

Fig. 14. Measured and calculated S-parameters of DGMESFET at bias point P_3 given in Fig. 3 with port 1: gate 1 and port 2: drain.

error function defined by

$$EF = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\sum_{j=1}^{3}\sum_{j=1}^{3} W_{ij}\frac{|S_{ij}^{(m)} - S_{ij}^{(c)}|^2}{|S_{ij}^{(m)}|^2}} \tag{29}$$

where $S_{ij}^{(m)}$ is the measured S-parameters, $S_{ij}^{(c)}$ is the calculated S-parameters, W_{ij} is the weighting factors, and N is the number of frequency points.

IV. Measurement Results

A coplanar DGMESFET with gate length 1 μm and gate width 4 $\times$ 75 μm for each gate, fabricated by HEXAWAVE Inc., is used to extract extrinsic and intrinsic elements of a small signal equivalent circuit based on the extraction formula described above. The wafer is probed by three GSG probes on a Cascade SUMMIT-9000 probe station. The dc transfer characteristics are given in Fig. 3.

A. DC End Resistance Measurement for Extracting Series Resistance Elements

DC end resistance measurements are conducted using an HP 4145B semiconductor parameter analyzer automated with a SUN Sparc-20 work station. Fig. 9 shows the measured results of $(\Delta V_{g1s})/(\Delta I_{g1s})$, $(\Delta V_{g1d})/(\Delta I_{g1d})$, $(\Delta V_{g2s})/(\Delta I_{g2s})$, and $(\Delta V_{g2d})/(\Delta I_{g2d})$ with drain terminal or source terminal floating and forward gate current ranging from 1–10 mA. They are shown in straight lines, with curves $(\Delta V_{g1s})/(\Delta I_{g1s})$ and $(\Delta V_{g2d})/(\Delta I_{g2d})$, $(\Delta V_{g2s})/(\Delta I_{g2s})$, and $(\Delta V_{g1d})/(\Delta I_{g1d})$ close together due to the device symmetry. The resulting values of series resistance extracted using (15)–(19) are listed as the initial values in Table I.

B. Cold Measurement for Extracting Inductance and Capacitance Elements

The three-port S-matrix of DGMESFET at bias $V_{g1s} < V_{th}\,(V_{th} = -1V)$, $I_{q2} = 1$ mA, and $V_{ds} = O$ V is measured from 2 to 6 GHz using an HP8510C with HP8511 frequency converter as a three-port network analyzer. Measured results of $\mathrm{Im}(Y_{11})$, $\mathrm{Im}(Y_{22})$, $\mathrm{Im}(Y_{21})$, and $\mathrm{Im}(Y_{33})$ are shown in Fig. 10. Extracted values of C_{pg1}, C_{pg2}, and C_{pd} using (20)–(24) are shown in Fig. 11. Fig. 12 shows the values of L_s, L_d, L_{g1}, and L_{g2} extracted using (25)–(28) from the S-matrix measurement with DGMESFET biased at $V_{DS} = O$ V, $I_{g1s} = I_{g2s} = 3$ mA. Both the capacitance and inductance values are shown independent of the operation frequency.

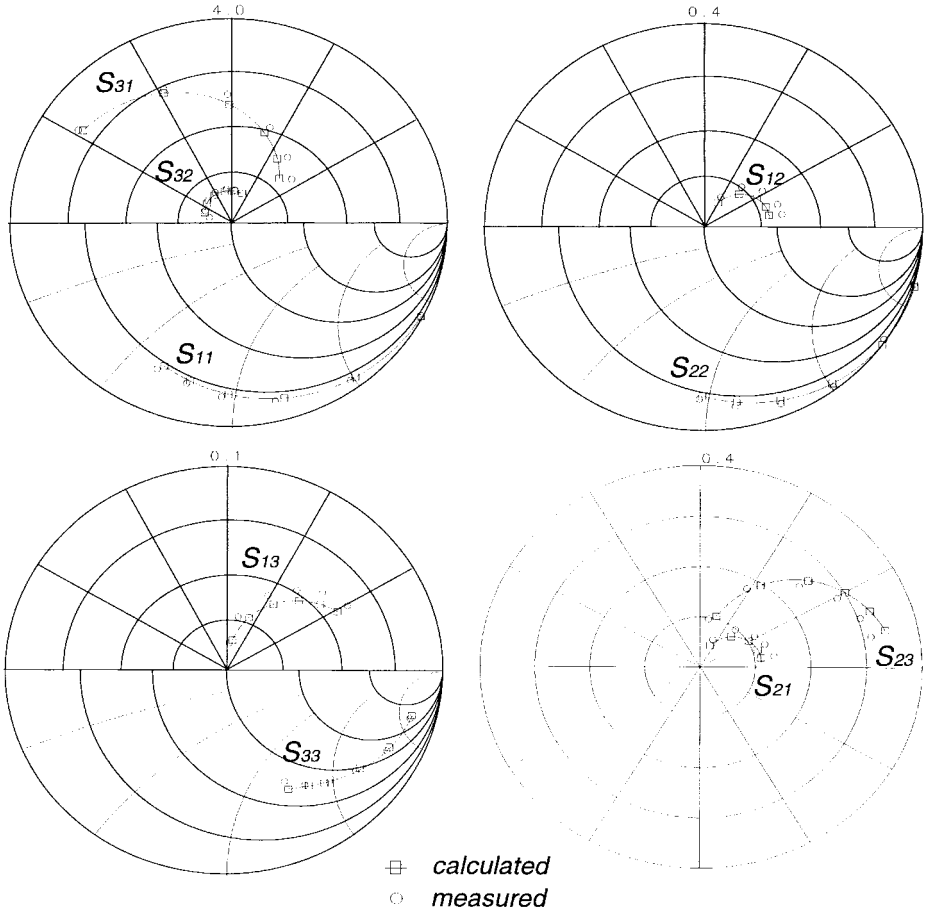

Fig. 15. Measured and calculated three-port S-matrix of DGMESFET at bias P_1 given in Fig. 3 with $V_{DS} = 5$ V, $V_{G1S} = -0.4$ V, and $V_{G2s} = 2$ V.

C. Hot Measurement for Extracting Intrinsic Elements and Optimization Results

As illustrated in Section II, two sets of two-port S-matrices are measured. One hot measurement is that the DGMESFET is biased at point P_2 given in Fig. 3. The intrinsic elements of FET2 are then extracted using (3)–(9). Fig. 13 shows the results of measured and calculated S-parameters of FET2. The calculated results are based on the equivalent circuit given in Fig. 4 using the extracted extrinsic and intrinsic values. They are shown in good agreement. The other hot measurement is to acquire the two-port S-matrix of DGMESFET at bias point P_3 given in Fig. 3 to extract the intrinsic elements of FET1. Fig. 14 shows the measured and calculated S-parameters.

The extracted values of extrinsic and intrinsic elements are then given as the initial values for the optimization calculation using HP/EEsof to fit the equivalent circuit given in Fig. 2 to the measured three-port S-matrix of DGMESFET biased at point P_1. The initial error function of (29) is less than 10%. This shows that the elements acquired using the developed extracted formula and the corresponding measurements can give a very closed result to the measured S-matrix. At the end of optimization using gradient search, the error function becomes less than 1% to indicate that a global minimum is reached. The measured and calculated three-port S-matrices from 1.5 to 11 GHz are given in Fig. 15. They are shown in a quite good agreement. Table I summarizes the initial values and final values of the extrinsic and intrinsic elements of DGMESFET.

V. Conclusions

A procedure for extracting the small signal equivalent circuit elements of DGMES-FET has been described. All the intrinsic and extrinsic elements are directly extracted from dc and RF measurements using analytical formulas. These values give about 10% error to the measured three-port S-matrix. This shows the extracted element values are quite accurate. They are then used as the initial values for optimization to acquire more accurate results. The results using the developed extraction formula shows that the described procedure gives a practical and accurate approach for DGMESFET characterization.

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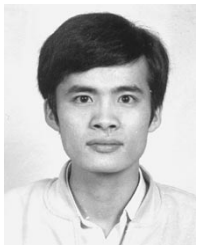
References

[1] S. Asai, F. Murai, and H. Kodera, "GaAs dual-gate Schottky-barrier FET's for microwave frequencies," *IEEE Trans. Electron Devices*, vol. ED-22, pp. 897–904, Oct. 1975.

[2] C. Tsironis and R. Meierer, "Microwave wide-band model of GaAs dual-gate MESFET," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 243–251, Mar. 1982.

[3] M. Schöön, "A novel, bias-dependent, small-signal model of the dual-gate MESFET," *IEEE Trans. Microwave Theory Tech.,* vol. 42, pp. 212–216, Feb. 1994.
[4] A. Madjor and J. Dreifuss, "Large-signal microwave performance prediction of dual-gate MESFET using an efficient and accurate model," *IEEE Trans. Microwave Theory Tech.,* vol. MTT-33, pp. 693–643, July 1985.
[5] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent-circuit," *IEEE Trans. Microwave Theory Tech.,* vol. MTT-36, pp. 1121–1129, July 1988.
[6] T. Furutsuka, M. Ogawa, and N. Kawamura, "GaAs dual-gate MESFET's," *IEEE Trans. Electron Devices,* vol. ED-25, pp. 580–586, June 1978.
[7] K. W. Lee, K. Lee, M. S. Shur, T. T. Vu, P. C. T. Roberts, and M. J. Helix, "Source, drain, and gate series resistances and electron saturation velocity in ion-implanted GaAs FET's," *IEEE Trans. Electron Devices,* vol. ED-32, pp. 987–992, May 1985.
[8] C. Tsironis and R. Meierer, "DC characteristics aid dual-gate FET analysis," *Microwaves,* pp. 71–73, July 1981.
[9] P. L. Hower and N. G. Bechtel, "Current saturation and small-signal characteristics of GaAs FET's," *IEEE Trans. Electron Devices,* vol. ED-20, pp. 213–220, Mar. 1973.



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